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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,852	06/25/2003	Kenneth C. Wu	ASC-022CPCN	3708

21323 7590 05/28/2004

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,852	WU ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *112-232* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☒ Claim(s) *See Continuation Sheet* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/03; 1/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims rejected are 112-139,144-154,156-158,163-165,171-176,179,180,183-187,198,199,201-207,212,213,215,218,221,222 and 229-231.
Continuation of Disposition of Claims: Claims objected to are 140-143,155,159-162,166-170,177,178,181,182,188-197,200,204,208-211,214,216,217,219,220,223-228 and 232.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: line 4 of page 13 requires that x is less than 18, which would mean that the SiGe alloy could possibly comprise $Si_{-16}Ge_{17}$, which does not seem to be the intent of the disclosure. Should this be 0.18?

Appropriate correction is required.

Claim Objections

Claim 118 is objected to because of the following informalities: In line 2, "etch stop" should be replaced with "etch-stop". Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 112 – 138, 144 – 150, 171, 172, 176, 179, 180, 199, 201 – 203, 205, 212, 213, 215, 218, 221, 222, 229, 230 and 231 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 9,

15, 24, 33, 37 – 42, 48, 89, 90, 94 and 97 of U.S. Patent No. 6,689,211. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the patent include each limitation of the instant application.

The claims of the instant application are considered to cite limitation of the claims of the patent as shown below, wherein the application claim number is on the left of the colon, and the corresponding patent claim on the right. Additional explanation follows.

(112 – 114: 1, 33), (115: 3), (116: 15, 48), (117: 24), (118: 33), (119: 37), (120: 48), (121: 5), (122: 7), (123: 6, 7, 8, 9), (124: 9), (125 – 127: 1), (128: 2), (129: 1, 3), (130: 1), (131: 5, 6), (132: 1), (133: 33), (134: 37), (135: 33, 37, 38, 40), (136: 37), (137, 138, 145, 147, 150: 33), (141: 48), (144: 33, 48), (146: 37), (148: 33, 37), (149: 37), (171, 172, 179, 180, 198, 201, 202, 203, 205, 212, 213, 221, 222, 229, 230, 231: 89), (176: 97), (218: 90, 94)

With respect to claim 112, claim 1 of the patent does not explicitly cite a semiconductor structure, but cites an etch-stop layer system for use on a silicon substrate, which is a semiconductor.

With respect to claim 121, claim 5 of the patent includes the limitation of bonding the etch stop layer to a second substrate, wherein the second substrate would have had no other purpose but that of a handle wafer.

With respect to claims 130, and 132 and similar claims relying on a layer being disposed over or under another layer, claims 1 and 33 of the patent do not specifically recite that the relaxed layer is disposed over the etch-stop layer. However, the relaxed layer being under or over the etch-stop layer is dependent upon the orientation of the device, which may be operated in any orientation.

With respect to claims 133 and 137, claim 33 of the patent does not specifically recite that the strained layer is over the uniform etch-stop layer. However, the strained

layer being over or under the uniform etch-stop layer is dependent upon the orientation of the device, which may be operated in any orientation. Additional claims with regard to a layer above or below another layer have been treated in the same manner.

With respect to claim 135, claims 33, 38 and 40 of the patent includes the limitation of bonding the etch stop layer to an insulative substrate, wherein the insulative substrate would have had no other purpose but that of a handle wafer.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 135 and 183 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent No. 5,013,681 to Godbey et al.

Regarding claim 135, Godbey et al. teaches a semiconductor structure (Fig. 3, for example), comprising:

a layer structure including a strained $Si_{1-z}Ge_z$ layer (24; Col. 3, lines 13 – 17); and

a handle wafer (30, 29) comprising an insulator, the layer structure being bonded to the handle wafer (Col. 4, lines 20 – 24),

wherein $0 \leq z < 1$ (Col. 3, lines 50 – 52).

Regarding claim 183, Godbey et al. teaches a method for forming a semiconductor structure (Fig. 3, for example), comprising:

forming a layer structure by forming a strained $Si_{1-z}Ge_z$ layer (24; Col. 3, lines 13 – 17), and

bonding the layer structure to a handle wafer (Col. 4, lines 20 – 24) comprising an insulator (32),

wherein $0 \leq z < 1$ (Col. 3, lines 50 – 52).

6. Claims 112 – 115, 117 – 125, 130 – 132, 135 – 139, 144 – 148, 150 – 154, 156 – 158, 163 – 165, 171 – 176, 183 – 187, 198, 199, 201 – 203 and 205 – 207 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,906,951 to Chu et al.

Regarding claim 112, Chu et al. teaches a semiconductor structure (Fig. 2) comprising:

a layer structure including a uniform etch-stop layer (14).

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 113, Chu et al. teaches a semiconductor device, wherein the uniform etch-stop layer is relaxed.

Regarding claim 114, Chu et al. teaches a semiconductor device, wherein the uniform etch-stop layer comprises $Si_{1-y}Ge_y$.

Regarding claim 115, Chu et al. teaches a semiconductor device, wherein $y>0.19$.

Regarding claim 117, Chu et al. teaches a semiconductor device, wherein the surface of the etch stop layer is planarized.

Regarding claim 118, Chu et al. teaches a semiconductor device, wherein the layer structure comprises a strained layer (16, 17) disposed over the uniform etch stop layer.

Regarding claim 119, Chu et al. teaches a semiconductor device, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

Regarding claim 120, Chu et al. teaches a semiconductor structure, further comprising an insulator layer (28) over the layer structure.

Regarding claim 121, Chu et al. teaches a semiconductor structure further comprising:

an additional wafer (26),

wherein the layer structure is bonded to the additional wafer (Col. 3, lines 20 – 25).

With respect to the requirement of the additional wafer being used as a handle wafer, this is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

Regarding claim 122, Chu et al. teaches a structure, wherein the handle wafer comprises an insulator (28).

Regarding claims 123 and 124, Chu et al. teaches a structure, wherein the additional wafer comprises silicon and silicon dioxide.

Regarding claim 125, Chu et al. teaches a structure, wherein the layer structure comprises a relaxed layer (18).

Regarding claim 130, Chu et al. teaches a structure, wherein the relaxed layer is disposed over the etch stop layer.

Regarding claim 131, Chu et al. teaches a structure, further comprising a semiconductor substrate (26) disposed over the relaxed layer.

Regarding claim 132, Chu et al. teaches a structure, wherein inverting the illustrated orientation of the embodiment in Fig. 2, would result in the relaxed layer (18) being disposed under the uniform etch-stop layer. Since the device can operate in any orientation, changing the orientation of the device to accommodate a plurality of applications does not amount to a change in the device structure.

Regarding claims 135 and 136, Chu et al. teaches a semiconductor structure, comprising:

a layer structure including a strained $Si_{1-z}Ge_z$ layer (16), and

an additional wafer (26, 28) comprising an insulator (28), the layer structure being bonded to the additional wafer (Col. 3, lines 20 – 25),

wherein z = 0, which falls inside of the range of $0 \leq z < 1$.

Regarding claim 137, Chu et al. teaches a semiconductor structure, wherein the layer structure includes a relaxed etch stop layer (14) disposed under the $Si_{1-z}Ge_z$ layer. Chu et al. further inherently teaches that the etch stop layer has a relative etch rate which is less than the relative etch rate of Si doped with $7x10^{19}$ boron atoms/cm^3, since the material is identical to that of the claimed invention.

With respect to the requirement of the additional wafer being used as a handle wafer, this is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

Regarding claim 138, Chu et al. teaches a semiconductor structure, wherein the etch-stop layer comprises relaxed $Si_{1-y}Ge_y$.

Regarding claim 139, Chu et al. teaches a semiconductor structure, wherein inverting the illustrated orientation of the embodiment in Fig. 2, would result in the relaxed layer (18) being disposed under the uniform etch-stop layer. Since the device can operate in any orientation, changing the orientation of the device to accommodate a plurality of applications does not amount to a change in the device structure.

Regarding claim 144, Chu et al. teaches a semiconductor structure, comprising:

a layer structure (Fig. 2) including:

a uniform etch-stop layer (14); and

a strained layer (16, 17) disposed over the uniform etch-stop layer, and

an insulator structure (28) over the layer structure.

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 145, Chu et al. teaches a structure, wherein the etch-stop layer comprises relaxed $Si_{1-y}Ge_y$.

Regarding claim 146, Chu et al. teaches a structure, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

Regarding claim 147, Chu et al. teaches a semiconductor structure, comprising:

an etch-stop layer (17); and

a substantially relaxed layer (18) over the etch-stop layer.

Regarding claim 148, Chu et al. teaches a structure, wherein the etch-stop layer comprises strained $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

Regarding claim 147, Chu et al. teaches a structure, wherein the relaxed layer comprises $Si_{1-w}Ge_w$.

Regarding claim 151, Chu et al. teaches a structure, comprising:

a first uniform etch stop layer (14);

a second etch stop layer (17) disposed over the uniform etch stop layer; and

a substantially relaxed layer (18) over the second etch stop layer.

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 152, Chu et al. teaches a structure, wherein the first etch stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

Regarding claim 153, Chu et al. teaches a structure, wherein the second etch stop layer comprises strained $Si_{1-z}Ge_z$.

Regarding claim 154, Chu et al. teaches a structure, wherein $0 \leq z < 1$.

Regarding claim 156, Chu et al teaches a structure, wherein the relaxed layer comprises $Si_{1-w}Ge_w$.

Regarding claim 157, Chu et al. teaches a structure, further comprising:

an additional wafer (26) comprising an insulator (28),

wherein the relaxed layer is indirectly bonded to the additional wafer.

With respect to the requirement of the additional wafer being used as a handle wafer, this is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

Regarding claim 158, Chu et al. teaches a structure, wherein the additional wafer (handle wafer) comprises silicon.

Regarding claim 163, Chu et al. teaches a method of forming a semiconductor structure, comprising:

forming a uniform etch stop layer (14);

providing an additional wafer (26, 28); and

indirectly bonding the uniform etch stop layer to the additional wafer.

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

With respect to the requirement of the additional wafer being used as a handle wafer, this is considered a suggested use limitation and is not given any patentable weight.

Regarding claim 164, Chu et al. teaches a method, wherein the uniform etch stop layer comprises relaxed $Si_{1-y}Ge_y$.

Regarding claim 165, Chu et al. teaches a method, further comprising planarizing the uniform etch-top layer prior to bonding. This can be seen in figure 2, where the p doped SiGe layer is grown directly on the surface of the uniform etch stop layer, which is clearly planarized. Since the layer structure is completed before the bonding step, the planarization would have necessarily been accomplished prior to bonding.

Regarding claim 171, Chu et al. teaches a method for making a semiconductor structure (Fig. 2), the method comprising:

providing a first substrate (12); and

forming a layer structure over the first substrate by:

forming a uniform etch stop layer (14) over the first substrate; and

forming a strained layer (17) over the uniform etch stop layer,

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 172, Chu et al. teaches a method, wherein the etch stop layer comprises relaxed $Si_{1-y}Ge_y$.

Regarding claim 173, Chu et al. teaches a method, wherein the strained layer comprises $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

Regarding claim 174, Chu et al. teaches a method, further comprising:

providing a second substrate (28, 26); and

bonding the layer structure to the second substrate (Col. 3, lines 20 – 25).

Regarding claim 175, Chu et al. teaches a method, wherein the second substrate comprises silicon.

Regarding claim 176, Chu et al. teaches a method, further comprising:

forming an insulator layer (28) over the strained layer.

Regarding claim 183 and 184, Chu et al. teaches a method for forming a semiconductor structure, the method comprising:

forming a layer structure by forming a strained $Si_{1-z}Ge_z$ layer (16), and

bonding the layer structure to a second wafer (26, 28; Col 3, lines 20 – 25) comprising an insulator,

wherein $z = 0$, which falls into the range of $0 \leq z < 1$.

With respect to the requirement of the additional wafer being used as a handle wafer, this is considered a suggested use limitation and is not given any patentable weight.

Regarding claim 185, Chu et al. teaches a method, wherein forming the layer structure, comprises forming a uniform etch stop layer (14) and the strained layer (16) is formed over the etch stop layer.

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$ boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 186, Chu et al. teaches a method, wherein the uniform etch stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

Regarding claim 187, Chu et al. teaches a method, further comprising:

forming an insulator (28) over the layer structure.

Regarding claim 198, Chu et al. teaches a method for forming a semiconductor structure, the method comprising:

forming a strained etch stop layer (17); and

forming a substantially relaxed $Si_{1-w}Ge_w$ layer (18) over the etch stop layer.

Regarding claim 199, Chu et al. teaches a method, wherein the etc-stop layer comprises $Si_{1-z}Ge_z$, and wherein $0 \leq z < 1$.

Regarding claim 201, Chu et al. teaches a method for forming a semiconductor structure, comprising:

forming a first uniform etch stop layer (14);

forming a second etch-stop layer (15, 17) over the uniform etch stop layer; and

forming a substantially relaxed layer (18) over the second etch-stop layer;

Chu et al. inherently teaches that the uniform etch-stop layer has a relative etch rate which is less than approximately the relative etch rate of silicon doped with $7x10^{19}$

boron atoms/cm^3, since the etch-stop layer of Chu et al. is identical to that of the instant application.

Regarding claim 202, Chu et al. teaches a method, wherein the first etch stop layer comprises substantially relaxed $Si_{1-y}Ge_y$.

Regarding claim 203, Chu et al. teaches a method, wherein the second etch stop layer (17) comprises strained $Si_{1-z}Ge_z$ and $0 \leq z < 1$.

Regarding claim 205, Chu et al. teaches a method, wherein the relaxed layer comprises $Si_{1-w}Ge_w$.

Regarding claim 206, Chu et al. teaches a method, further comprising:

indirectly bonding the substantially relaxed layer to a substrate (26, 28) comprising an insulator (col. 3, lines 20 – 25).

Regarding claim 207, Chu et al. teaches a method, wherein the substrate comprises silicon.

Allowable Subject Matter

7. Claims 14 – 143, 155, 159 – 162, 166 – 170, 177, 178, 181, 182, 188 – 197, 200, 204, 208 – 211, 214, 216, 217, 219, 220, 223 – 228 and 232 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Chu et al. does not teach a device as claimed, and including an etch stop layer comprising substantially relaxed graded $Si_{1-x}Ge_x$.

The prior art of record does not teach a device with a handle wafer comprising an insulator and an insulator disposed over the layer structure.

The prior art of record does not teach a uniform etch stop layer, wherein a uniform etch stop layer with a relative etch rate which is less than Si doped with $7x10^{19}$ boron atoms/cm^3 comprises $Si_{1-z}Ge_z$, and $z=0$.

The prior art of record does not teach removing a portion of the uniform etch stop layer.

The patent claims do not recite a method including bonding the substantially relaxed layer to a substrate.

The patent method does not recite a second etch stop layer comprising a strained $Si_{1-z}Ge_z$, wherein $0 \leq z < 1$.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens
Patent Examiner